What is claimed is:

1. An emulator for verifying a logic design of a target chip to be mounted in a target system, comprising:

a processing engine (PE) for executing a software algorithm corresponding to the logic design of the target chip, said software algorithm having at least one software variable defined therein; and

a target interface engine interfacing with said target system for transmitting/receiving pin signals to/from said target system in response to the execution of said software algorithm by said processing engine,

wherein said at least one software variable and said pin signals are time-variant and said processing engine includes means for finding correspondence between said at least one software variable and said pin signals at a predetermined time.

2. The emulator according to claim 1, wherein said target interface engine comprises i) a pin signal generator for generating pin signals to be transmitted to said target system and receiving pin signals from said target system; and ii) a pin signal monitor for receiving and storing said pin signals communicated between said pin signal generator and said target system.

3. The emulator according to claim 2, wherein said pin signal monitor further stores time information associated with said pin signals.

4. The emulator according to claim 3, wherein said pin signal monitor comprises a trigger event detector for detecting an occurrence of a first trigger event defining a case where values of said pin signals meet a predetermined condition.

5. The emulator according to claim 4, wherein said trigger event detector further comprises means for transmitting a first interrupt request signal to said processing engine in response to the occurrence of said first trigger event.

6. The emulator according to claim 5, wherein said predetermined time is associated with the time when said first trigger event occurs.

7. The emulator according to claim 6, wherein said processing engine includes a software variable monitor for monitoring said at least one time-varying software variable and controlling values of the monitored software variables to be stored.

8. The emulator according to claim 7, wherein said software variable monitor is a software routine which is inserted into said software algorithm.

9. The emulator according to claim 7, wherein said processing engine further comprises a software variable buffer for storing said values of the monitored software variables.

10. The emulator according to claim 9, wherein said

software variable buffer further stores time information associated with said values of the monitored software variables.

11. The emulator according to claim 10, wherein said processing engine responds to said first interrupt request signal after a predetermined wait time lapses from the timing when said first interrupt request signal is transmitted by said first interrupt request signal transmitting means, and wherein said software variable buffer has a buffer capacity such that it could store all the changes in said monitored software variables during said predetermined wait time.

12. The emulator according to claim 10, wherein said processing engine further comprises a pin signal buffer and means for controlling the storing of pin signals which have been stored in said pin signal monitor in said pin signal buffer in response to said first interrupt request signal.

13. The emulator according to claim 9, wherein said software variable monitor further comprises means for detecting an occurrence of a second trigger event defining a case where values of said time-varying software variables meet a predetermined condition.

14. The emulator according to claim 13, wherein said software variable monitor further comprises means for outputting a second interrupt request signal in response to the occurrence of said second trigger event.

15. The emulator according to claim 14, wherein said processing engine further comprises means for controlling the storing of pin signals which have been stored in said pin signal monitor in said pin signal buffer in response to said second interrupt request signal.

16. The emulator according to claim 12 or claim 15, wherein said processing engine further includes a variable/signal analyzer for analyzing the progress or error during emulation by using information stored in said software variable buffer and said pin signal buffer.

17. An emulator for verifying a logic design of a target chip to be mounted in a target system, comprising:

a processing engine (PE) for executing a software algorithm corresponding to the logic design of the target chip, said software algorithm having at least one software variable defined therein; and

a target interface engine interfacing with said target system for transmitting/receiving pin signals to/from said target system in response to the execution of said software algorithm by said processing engine,

wherein said at least one software variable and said pin signals are time-variant, said processing engine comprises a first means for tracking time-varying changes in said at least one software variable, and said target interface engine comprises a second means operatively coupled to said first means for tracking time-varying

changes in said pin signals.

18. The emulator according to claim 17, wherein said target interface engine further comprises a pin signal generator for generating pin signals to be transmitted to said target system and receiving pin signals from said target system and said second means comprises a pin signal monitor for receiving and storing said pin signals communicated between said pin signal generator and said target system.

19. The emulator according to claim 18, wherein said pin signal monitor further stores time information associated with said pin signals.

20. The emulator according to claim 19, wherein said pin signal monitor comprises a trigger event detector for detecting an occurrence of a first trigger event defining a case where values of said pin signals meet a predetermined condition.

21. The emulator according to claim 20, wherein said trigger event detector further comprises means for transmitting a first interrupt request signal to said processing engine in response to the occurrence of said first trigger event.

22. The emulator according to claim 21, said first means comprises a software variable monitor for monitoring said at least one time-varying software variable and controlling values of said monitored software variables to be stored.

23. The emulator according to claim 22, wherein said software variable monitor is a software routine which is inserted into said software algorithm.

24. The emulator according to claim 22, wherein said first means further comprises a software variable buffer for storing said values of the monitored software variables.

25. The emulator according to claim 24, wherein said software variable buffer is controlled to further store time information associated with said values of the monitored software variables.

26. The emulator according to claim 25, wherein said first means responds to said first interrupt request signal after a predetermined wait time lapses from the timing when said first interrupt request signal is transmitted by said first interrupt request signal transmitting means, and wherein said software variable buffer has a buffer capacity such that it could store all the changes in said monitored variables during said wait time.

27. The emulator according to claim 25, wherein said first means further comprises means for controlling the storing of pin signals which have been stored in the said pin signal monitor in said pin signal buffer in response to said first interrupt request signal.

28. The emulator according to claim 24, wherein said software variable monitor further comprises means for detecting an occurrence of a second trigger event defining a

case where values of said time-varying software variables meet a predetermined condition.

29. The emulator according to claim 28, wherein said software variable monitor comprises means for outputting a second interrupt request signal in response to the occurrence of said second trigger event.

30. The emulator according to claim 29, wherein said first means comprises means for controlling the storing of pin signals which have been stored in said pin signal monitor in said pin signal buffer in response to said second interrupt request signal.

31. The emulator according to claim 27 or 30, wherein said first means further includes a variable/signal analyzer for analyzing the progress or error during emulation by using information stored in said software variable buffer and said pin signal buffer.

32. A method for verifying a logic design of a target chip to be mounted in a target system, comprising the steps of:

executing a software algorithm corresponding to the logic design of the target chip, said software algorithm having at least one software variable whose value is time-variant with the execution of said software algorithm;

generating pin signals to be transmitted to said target system in response to the execution of said software algorithm, the values of said pin signals being time-variant with the execution of said software algorithm; and

providing a temporal history for changes in said at least one software variable and said pin signals.

33. The method according to claim 32, wherein said step of providing a temporal history comprises recording changes in said at least one software variable with respect to time.

34. The method according to claim 32, wherein said step of providing a temporal history comprises recording changes in said pin signals with respect to time.

35. The method according to claim 34, further comprising a step of detecting an occurrence of a first trigger event defining a case where values of said pin signals meet a predetermined condition.

36. The method according to claim 35, further comprising a step of generating a first interrupt request signal in response to the occurrence of said first trigger event.

37. The method according to claim 33, further comprising a step of detecting an occurrence of a second trigger event defining a case where values of said time-varying software variables meet a predetermined condition.

38. The method according to claim 37, further comprising a step of outputting a second interrupt request signal in response to the occurrence of said second trigger event.

39. The method according to claim 36 or 38, further comprising a step of referencing said temporal history in response to the occurrence of either said first interrupt

request signal or said second interrupt request signal.

40. An emulator for verifying a logic design of a target chip to be mounted in a target system, comprising:

means for executing a software algorithm corresponding to the logic design of the target chip with at least one software variable present in said software algorithm and for transmitting/receiving pin signals to/from said target system in response to the execution of said software algorithm, wherein said at least one software variable and said pin signals are time-variant with the execution of said software algorithm; and

means for recording changes in said at least one software variable and said pin signals with respect to time for a predetermined period of time.